

A Virtual Interactive Teaching Environment (VITE)

Using XML and Augmented Reality

Martin White, Emmanuel Jay, Fotis Liarokapis, Costas Kostakis, Paul Lister

Centre for VLSI and Computer Graphics,

University of Sussex, Falmer, Brighton,

BN1 9QT, England, UK

Email: M.White@sussex.ac.uk

Abstract

We present a new approach to the teaching of top down design of VHDL using a novel Virtual Interactive Teaching Environment. This environment enables students to learn more effectively using virtual multimedia content, while exploiting XML, and augmented reality. This environment can be adapted for teaching of other subject areas.

Keywords: Augmented Reality, Virtual Environments, XML, VHDL, Electronic Design Automation.

1 Introduction

At Sussex, in the School of Engineering and Information Technology, we teach top down design with VHDL to the 4th year MEng Electronics and Computer Systems majors on a course called Integrated Circuit Design 2 (ICD2)—our Integrated Circuit Design 1 being the VLSI Systems full custom course using ChipWise. We also teach it on our MSc in Digital Electronics as half of the VLSI ASIC Design Module—the other half, again covering full custom design, but with L-EDIT. On the ICD2 course we use industry leading Electronic Design Automation (EDA) tools.

The EDA tools we use are ModelSim from Model Technology, which is used for simulation, Synplify from Synplicity, which is used for synthesis, etc. and Max+plus II from Altera, which is used for placing and routing the Altera FPGAs. We are also evaluating Renoir from Mentor Graphics to allow graphical design entry in our chosen top down design flow.

Our teaching of top down design with VHDL is delivered through seminars and laboratories focused on a self-based learning approach using multimedia tools from Esperan [1]. This paper presents a new teaching and learning virtual environment called VITE that uses XML and Augmented Reality to enhance our current teaching and learning model. Using VITE students can visualise principles and test their learning in virtual scenarios.

2 Our Current Teaching Model

Our current teaching model is illustrated in Figure 1, and is based around delivering:

- A 3-hour interactive seminar to introduce students to the course.
- A 1-hour demonstration of EDA tools including the specific design flow used.
- 11 to 12 hours completing the Esperan Multimedia HDL tutorials. There are 10 laboratory exercises included in the tutorials.
- 15 hours completing the design exercise, which is assessed. Students have to submit a 4000-word report inclusive of diagrams and results, and a short essay.

The core of our teaching model is focused on a self-based learning approach using the Esperan MasterClass tutorial. We feel this is appropriate for several reasons. First, the class is small, approximately 10 students. Second, the students are 4th year MEng level and capable of self-direction to a large extent. Third, because the class is small and predominantly laboratory based the teacher and laboratory demonstrators can almost interact on a one-to-one basis in support. The reader should note that although the class is small we still insist on 2 demonstrators and a teacher during the laboratories because the EDA tools are quite complex. Finally, the EDA tools are industry standard and we wanted to compliment this with an industry standard VHDL teaching package; this is the Esperan Multimedia HDL tutorials, which is normally delivered as an industry Master Class over 3 days.

We can see from Figure 1 that the students are set-up during the seminar before starting the self-based learning with MasterClass. There are 10 laboratory exercises in the MasterClass and the students are encouraged to cover at least the first 6, by which time they are reasonably familiar with simple VHDL concepts and the EDA tools. The teacher and laboratory demonstrators are on hand to provide support.

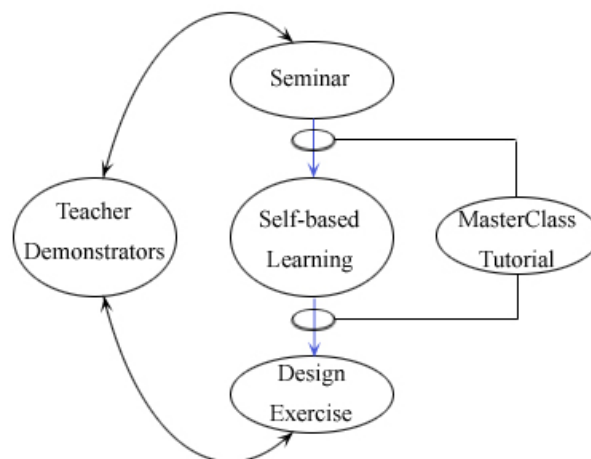


Figure 1 Our current teaching model

2.1 Seminar

During the seminar the students are introduced to the following material:

- Course introduction
- High Level Design with VHDL
- Introduction to VHDL
- Finite State Machine Design with VHDL
- A Practical VHDL Based Design Flow
- Design Assignment

2.1.1 Course Introduction

During the seminar the students are introduced to all the teaching material they will use during the course. The students are issued with the course introduction sheets, which details in brief what they will encounter during the course, and the relevance of each topic is explained, see discussions below. The Esperan MasterClass Multimedia HDL tutorial package is issued to each student, signed for, and discussed. The students are allowed to use this at home. The Altera UP1 FPGA board is shown and discussed.

2.1.2 High Level Design with VHDL

A 1-hour presentation on high level design with VHDL is given to introduce the students to the basic concepts they need to acquire during the laboratory session. This presentation covers typical ASIC and FPGA based top down design flows using VHDL, comparison of schematics versus VHDL, other design methodologies and abstraction, basic VHDL concepts and application areas. We discuss each stage of the design flow: specification, partitioning, design entry, simulation, synthesis, and optimisation. It finishes with a closer look at VHDL—an illustration of a structural VHDL 3 bit adder subtractor is given—and the practical VHDL based design flow the students will use.

The student is also given a set of notes for reference material to supplement the presentation, which describes the concept of high level or top down design with VHDL. This provides focused reading material for the student to research around as part of the assessment.

2.1.3 Introduction to VHDL

We do not focus on teaching VHDL in lectures; rather we adopt a self-learning approach based on Esperan's MasterClass Multimedia HDL tutorial. However, to supplement the MasterClass HDL tutorials we have developed a set of reference notes titled 'Introduction to VHDL'. These reference notes do not cover all aspects of VHDL that may be found in a

good VHDL textbook such as ‘VHDL for Designers’ [2]. But enough VHDL is covered to master the basics needed to complete the course, keeping in mind a major objective is to understand top down design, and not to produce expert VHDL programmers. We cover for example: language abstraction, hierarchy, VHDL components, VHDL entity and architecture, concurrent VHDL, sequential VHDL, and structural VHDL.

We believe this to be necessary because as good as the Esperan multimedia tutorial is, not all students have computing access at home to use the multimedia tutorial, and some students prefer more traditional learning approaches.

2.1.4 Finite State Machine Design with VHDL

For reference and to remind the students about finite state machine theory we provide a set of notes that cover the design of finite state machines and their implementation in VHDL. This also serves to illustrate other VHDL coding styles. The FSM can be implemented as a one, two or three process statement model for example. The student is encouraged to study this reference material because it is highly relevant to the design assignment. The notes first define the concepts of **combinatorial** and **sequential** logic (obviously revision material), **state**, **state transition**, **present state** and **next state** in the context of a diagram illustrating the synchronous sequential logic machine. Mealy and Moore FSMs are discussed in the context of state diagrams and state transition tables. An example of a Mealy and Moore FSM is given, and a two-process statement VHDL description of each is illustrated. This provides a model, which can be adapted for the design assignment. We go on to discuss microcoded state machines and simple microprogramme controller design for interest.

2.1.5 A Practical VHDL Based Design Flow

The top down design flow used by the students is illustrated in Figure 2. Currently we use three main EDA tools: Modelsim, Synplify and Max+plus II. Because the class is relatively small and well resource it is not uncommon for most if not all the students to reach the stage of programming the FPGA on the Altera UP1 board.

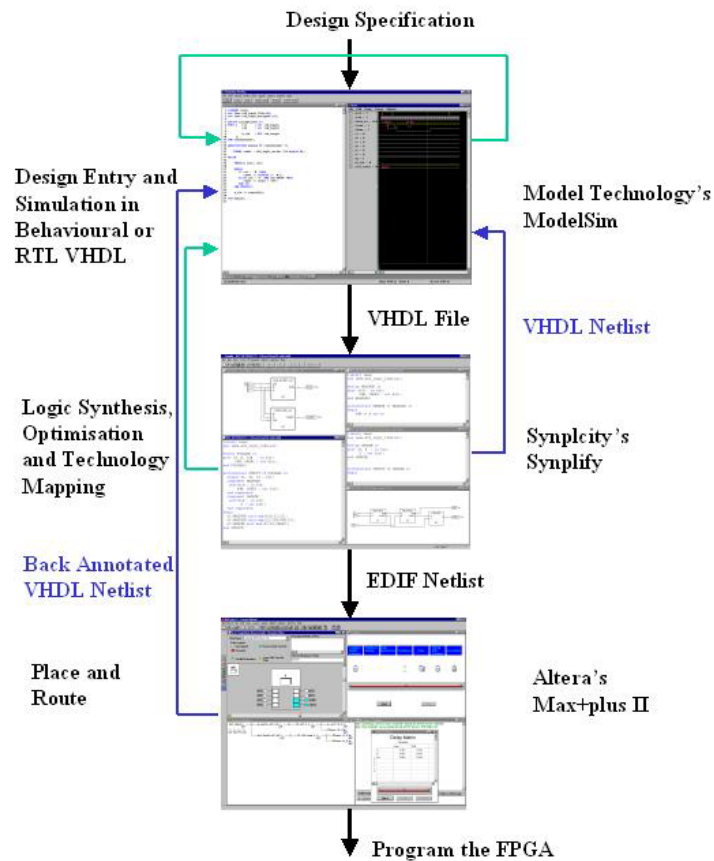


Figure 2 Top down design flow

2.1.6 Design Assignment

The assessed exercise is based around designing a simple digital component, which can be programmed into the Altera UP1 board. To provide depth to the exercise we ask the student to design the component in two different ways: first as a Mealy or Moore FSM (Finite State Machine) using the VHDL FSM coding principles outlined in the seminar and reference notes, and second using structural VHDL.

The designs are slightly more complicated in that the student has to also make sure the design can be implemented on the Altera UP1 board. This in effect means that the counter output has to be decoded for display on the seven segment displays, and the Altera UP1 board 25 MHz clock frequency has to be divided down. This usually leads to three components in the structural design: clock divider, counter, and the decoder, but also leads to some interesting VHDL code in the FSM approach. Does the student use one, two, or three process statements? How should the clock signal and decoding logic be handled?

2.1.7 Improvements

Although this course has run successfully for several years now, we still seek to improve the learning experience and increase understanding of the top down design with VHDL methodology. How can this be done? Looking at Figure 1 again, we feel that our approach is successful to a large extent, particularly the use of multimedia tutorials and the use of industrial EDA tools. Thus, logically we need to look at how the self-learning approach can be enhanced perhaps in conjunction with the design exercise. The rest of this paper focuses on how Virtual Reality, in particular Augmented Reality, can be applied in a virtual electronic design environment to enhance the students learning experience, and which compliments the industry standard top down design flow we have adopted.

3 Augmented Reality

Augmented Reality (AR) is one of the most promising areas of *Virtual Reality (VR)* or *Virtual Environments (VE)*. Using a typical VR system a user can move and interact within a computer-simulated environment commonly referred to as a virtual environment. VE technologies immerse a user inside a synthetic environment. In contrast, AR's main characteristic is that it enhances information, from the real world using computer-generated objects, onto the user's world-view. The ideal AR system will be able to compose computer-generated images or videos with the real world in real time in such a way that the user cannot tell the difference. Vallino states, "An augmented reality system could be considered the ultimate immersive system. The user cannot become more immersed in the real world" [3]. On the other hand the two most important drawbacks that current AR systems face, concern robust registration of the real world with the virtual world in real time and accurate sensing of the user in the real world—both the subject of current research efforts.

Advances in computer technology in recent years has facilitated the study of augmented reality systems and evolved many new applications on a variety of application domains. Typical applications in which AR has been applied are: *manufacturing, maintenance and repair, medical, military, collaborative interior design, entertainment, cultural heritage and fashion design.*

One of the earliest applications of AR is in military training of helicopter pilots. Using specially designed head mounted displays (HMDs) graphical navigation and flight information is superimposed upon the pilot's view of the real environment during the flight [4]. Another example of using AR is for live training concerning ground combat vehicles. This simulation was performed interactively and allowed the soldiers to see virtual objects (vehicles) on a virtual simulated battlefield [5].

Given the success of AR so far, we would like to consider how AR could benefit teaching and learning of the top-down design methodology. The need emerges because classroom instruction is sometimes insufficient, the design methodology is complex, and often limits the range of experience [6]. However, before we consider using AR to support teaching and learning of top down design flows, let us look first at the concepts behind virtual design.

3.1 Virtual Design

We have recently proposed an approach to virtual product design, and virtual design teaching called the Virtual Design Educator (VDE) [7], which outlined a generic virtual design methodology, and showed the potentials of virtual reality technology both in a teaching and an industrial context. In particular the VDE defined four main generic design dependencies: a design depends on time constraints, industry needs, the application it is aimed at, and human factors that influence the design.

In such a virtual approach, human factors are also related to the technology itself, and the way it is used as an interface between the real and the virtual world. These key areas will affect the outcome of the design, and need to be considered in a design education context. The VDE also emphasises that virtual reality technology needs to be carefully introduced into the teaching environment. A quick, unsubtle, introduction of technology into an already overcrowded curriculum may well slow down the teaching and learning process. Indeed, it could be said that our current EDA tools are highly complex, and the design flow used is difficult for the student to grasp in a 30-hour curriculum. Therefore, the introduction of yet more technology—Augmented Reality—needs to be carefully implemented for its use to be perceived in a positive way by the students.

For electronic design it is important to have the opportunity to test several design solutions. For example, a PC motherboard requires the integration of many experts to design each single component, and also to integrate them all on the board. Each team of experts will provide individual contributions on their own specific components. In such a complex application a change in one component may induce a series of dramatic change for all the other teams. Virtual reality technologies can help in sufficiently reducing the complexity introduced by such change.

3.2 Potential Benefits

When investigating the potential benefits of using an AR system in a teaching and learning environment we are considering two issues: the effect it has on the teaching and learning process, and the consequence of introducing new advanced technology in the classroom. Considering this some potential benefits are:

- Provision of tools that enable the fast and efficient generation and dissemination of learning material, and a set of virtual scenarios and support materials that students can control and interact with.

- Provision of virtual multimedia course notes that are particularly interesting and stimulating, as they can be immediately made available in the virtual environment. Students can build their own presentations.
- Reduction of printed material, although the option for the student to print out a presentation could exist.
- Simplify the teacher's task in providing much more stimulating teaching materials.
- Enables team working, which is essential when working in industry. Developing team skills is an essential part of the learning process

3.3 Technological Issues

It is important to consider the technological issues when introducing AR to the teaching and learning process. For example, the system must:

- Be simple and robust.
- Provide the user with clear and concise information.
- Enable the teacher to input information in a simple and effective manner.
- Enable easy interaction between users.
- Make complex procedures are transparent to the user.
- Be cost effective.

Ideally, such system should be built from off-the-shelf components, thereby reducing costs. It is generally accepted that a major reason for using virtual technology is related to costs. Is it better to buy AR hardware, and have the possibility to use virtual books, virtual hardware, or buy the actual physical books or hardware? VITE aims to find the solution to this question.

3.4 Exploiting AR

A carefully planned and managed presentation of AR technology is needed to avoid the teaching and learning environment being solely focussed on technological issues rather than educational ones. This careful planning and use of AR technology will then lead to an improvement in the teaching and learning process [7].

This issue is of particular importance, as students will most certainly need to adapt to the way AR hardware is used. This phase of the learning process needs to be short and well planned in the teaching model. It can also provide additional stimulus for the students, and lead to a better understanding of the principles taught. Figure 3 shows the areas of our initial teaching model where AR will be used to improve teaching and learning.

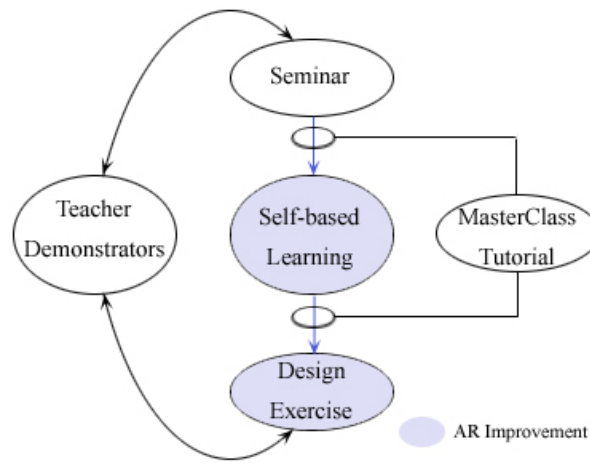


Figure 3 Areas where augmented reality could be used

In our current teaching model self-based learning consists of printed reference materials together with multimedia computer based tutorials—the Esperan MasterClass Multimedia HDL tutorial. This traditional way of presenting materials is widely used. As part of an augmented reality environment new means for presenting materials could be exploited. We refer to this new category of materials as *virtual multimedia content (VMC)*. Using VMC students can see real life three-dimensional examples of the principles they are studying.

4 Virtual Interactive Teaching Environment

Having consider augmented reality, virtual design, benefits, technology issues and where to exploit it, we propose an augmented reality environment called the **Virtual Interactive Teaching Environment (VITE)**, which is aimed at improving the teaching of electronic systems design. The benefits of using AR are clear for applications related to, for example, manufacturing, military and entertainment, see section 2. In a teaching context, AR can be used to help students understand principles, test designs in a virtual context, or provide students with additional support scenarios.

4.1 The VITE Teaching Model

VITE exploits a horizontal teaching model as opposed to a vertical teaching model. We define vertical teaching models as being specific to one discipline, e.g. teaching methods in an engineering context, see Figure 4. Here we see that the subject taught is defined as vertical because a single teacher would coordinate lectures, workshops and laboratories based around a single subject. Example subjects might be the teaching of Java programming, or VHDL or business studies. Thus, vertical models are defined for specific subjects, and are often different depending on the teacher, with different environments for each subject.

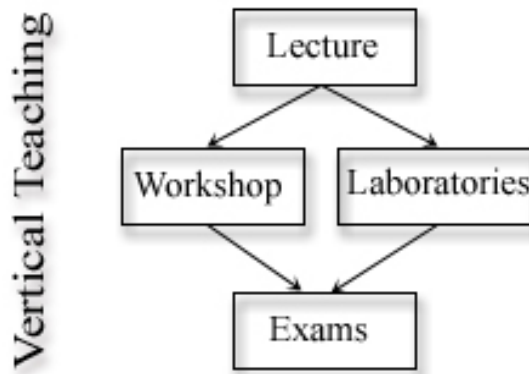


Figure 4 Vertical teaching model

We define horizontal teaching models as being more flexible allowing not only the teaching of single subject areas but also for cross-disciplinary teaching. For example, we may wish to teach top down design with VHDL with this horizontal teaching model, but allow the option to access teaching media from other related disciplines. This would be ideal for implementing a group project that required software, hardware and a business approach taught concurrently. Our horizontal model is aimed at the broader teaching community, and is rendered possible by virtual technologies such as augmented reality. In other words, AR technology provides a common cross-disciplinary and interactive environment for teaching, see Figure 5

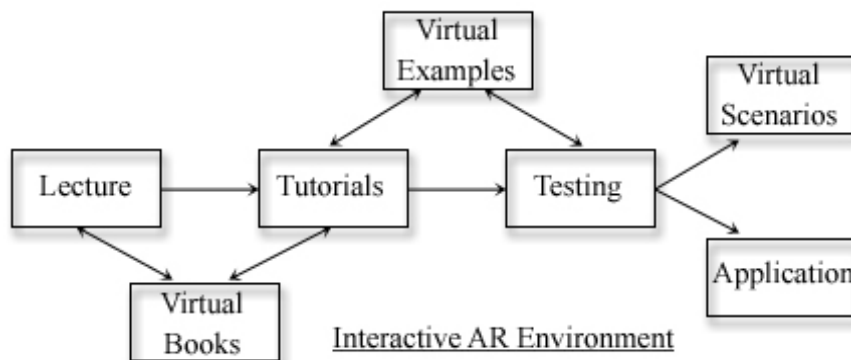


Figure 5 Horizontal teaching model

The horizontal teaching approach is particularly interesting as it enables the generic definition of teaching modules that can be easily re-used for other disciplines. For example, a VHDL module could be used in several different courses.

4.2 VITE Architecture

VITE is an AR teaching system that can provide teachers or trainers with 3D visualisations of teaching materials in an augmented reality environment, e.g. example designs, tutorials, 3D objects, reference manuals, etc.

Another aim of VITE is also to display virtual prototypes of typical target electronic systems, for example the **Altera UP1 board**, in real time. A high-performance PC with a high-performance graphics accelerator card will render the pre-generated 3D models to produce a virtual representation of the Altera UP1 board to be developed. In reality, we do not need to build a 3D model of the Altera UP1 board; we only need to virtually represent the components of interest. The virtual modelling of the actual electronic system is beyond the scope of this paper, and has already been presented at the EEUG Sheffield workshop last September [8].

The effectiveness of VITE is based on many parameters concerning technological issues such as: choice of display systems, haptic and kinaesthetic devices, object and user tracking systems and auditory perception devices, and virtual multimedia issues such as: generation of augmented reality software, creation of a large database and three dimensional modelling. Effective implementation of these systems in VITE will allow real time interaction between users and the system.

4.2.1 User Interaction within VITE

VITE has to support communication and interaction between the users, i.e. the students and the teacher, within the virtual environment. The VMC, which is stored in a database and visualised on an appropriate medium, is the information interface between the AR technology and the users. The technology encompasses both the AR software/hardware and the existing EDA tools that operate within VITE, see Figure 6.

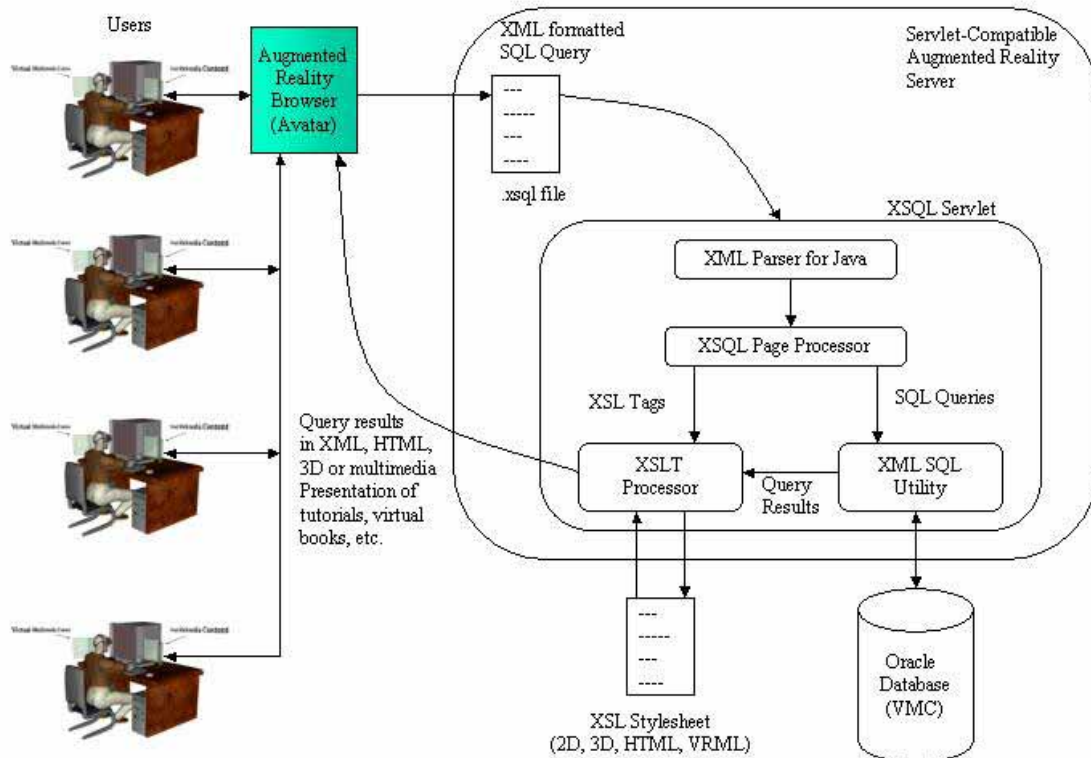


Figure 6 VITE system architecture adapted from the Oracle XML handbook [12]

We propose to implement an XML (Extensible Markup Language) meta-language based on a set of specially defined meta tags and appropriate XML schema or XML Data Type Definition [9] that defines the grammar of the language, which will be used by the teacher to add functionality to the VITE database. All functions necessary for the operation of VITE will be stored in a database such as Oracle, which has a set of XML development tools useful for the programming of the database, see the section 4.2.2 for a more detailed description of the database multimedia functionalities.

The database stores all the VMC information, as well as functionalities, which is input to VITE when required. For example, if a student requires a presentation on the top-down design methodology an XML formatted query on the database is generated and a top-down design methodology presentation is output from the database and displayed in the appropriate medium, e.g. 3D, or HTML. XML facilitates searching on elements within the database, thus more detailed database queries may result in accessing more specific information such as an explanation of logic synthesis.

Students will use existing EDA tools, e.g. ModelSim, Synplify and Max+plus II), concurrently with our VMC interface, as they were doing before. But, during the design and implementation practical sessions they will be able to interact with each other and VMC information in the database.

4.2.2 Database Multimedia Functionalities

The VITE architecture is particularly suited for teaching as it enables teachers to input information in an easy and powerful way. XML is now widely recognised as being the data description language of choice. Using XML non-programmers can easily describe data and information using custom and pre-defined tags. For example, there exists an already pre-defined set of XML tags called the Synchronised Multimedia Interface Language (SMIL) that describes multimedia content information and how to synchronise the information in a multimedia presentation [10]. We can adapt SMIL to describe part of the VMC information. Further, work is currently being done on X-VRML—the XML Virtual Reality Modelling Language—that can be adapted to describe the 3D and AR aspects of the VMC information [11].

The teachers existing material, i.e. the notes described in section 2.1 above, are now described in an XML file, with appropriate custom defined XML tags associated with all the different textual and pictorial descriptions or data, e.g. as a minimum each section of the notes would have an XML meta tag. This XML file is added to the database. XML style sheets are used to transform this data into specific 2D or 3D behaviour that will be performed on elements—text, pictures, multimedia objects, such as avatars, etc.—within the database.

This approach could also enable the teacher to build simple models out of basic elements within the database. Because each element corresponds to a XML meta tag, a new XML file can be generated from selected elements to make a new multimedia presentation within VITE. Thus, the database will typically consist of XML descriptions of 2D and 3D objects including behavioural information, text information, and voice data.

Our approach to data description using XML greatly simplifies the interaction between the teacher and the system. VITE provides the following major multimedia functionalities:

- Access to all relevant books, notes and other useful text, images or 3D objects that describe top down design.
 - The content is stored as XML descriptions in the database and visualised in 3D using XSL style sheets.
- Visualisation of ready-made electronic design models, rendered in real time in a realistic manner.
- Avatars to perform predefined or custom presentations and provide answers to a student queries.
- Tutorials on the use of the AR hardware, e.g. virtual displays, gloves, etc.
- Tutorials on the use of the AR software, which is responsible for robust registration and tracking.

4.3 Top Down Design with VHDL Example

As mentioned, we wish to improve the teaching of top down design using VHDL methodology. Students are required to design a simple digital component, see section 2.1.6. Using VITE the teaching and learning process, including the

Esperan Multimedia tutorials is delivered in an augmented reality environment where the student uses optical see-through glasses to switch their vision between the VMC information and the existing EDA tool design flows, see Figure 7.

The student will visualise in 2D and 3D all material, including the design assignment, together with the VHDL principles (notes, books, tips, etc.), which are overlaid in three dimensions in front of each student during all the laboratory sessions. Furthermore, avatars—an avatar is a graphical representation of a user, e.g. demonstrator, in the virtual environment that will respond to queries from the student—are used instead of demonstrators to illustrate examples, such as VHDL coding principles and other relevant information. The student can request information from the avatar that will initiate a dialog with the student to refine the question, see Figure 6. For example, the avatar may ask the student how they want to visualise the information, e.g. as 3D or as text. The avatar will then make an XML formatted query on the database, which is parsed into a set of XSL tags and an SQL query. The XSL tags select the appropriate style sheet that will translate the query results into the appropriate display medium, e.g. HTML on a browser, VRML in the AR display, or even simple text formatted for print. Further, there are several avatars dedicated to different queries.

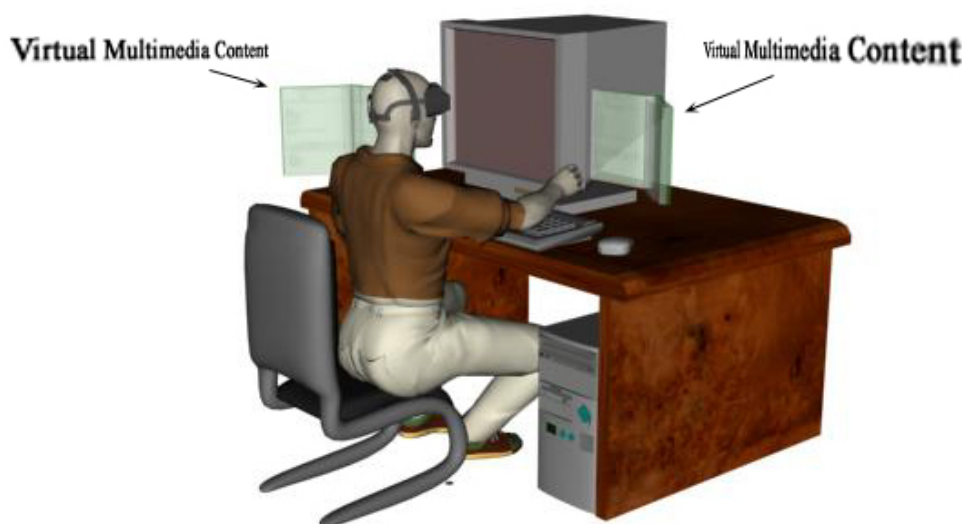


Figure 7 Augmented reality environment

More specifically, we can imagine the student depicted in Figure 7 is interacting with the EDA tools on the PC monitor and keyboard, while referencing tutorials and other supporting material, i.e. on the virtual screens beside him.

5 Conclusions

The augmented reality system presented is focused on enhancing the teaching and learning process. The example we describe is that of teaching top down design with VHDL, but other examples are applicable. It offers the teacher the ability to use more sophisticated techniques that enable better user interaction with teaching materials and complex EDA tools. It gives students a high degree of flexibility and understanding of the teaching materials by providing them in an

interactive and augmented way. We believe that a VE will provide a rewarding learning experience that is otherwise difficult to obtain [13].

Since real time interaction between users and material is a prerequisite it will facilitate rapid uptake of the concepts. Furthermore, we believe that more complex electronic system designs could be attempted that would be impossible to do with the current teaching methodology. The only disadvantage is the cost but our proposed system is much more cost effectiveness than a fully VR immersive system. The system that we are currently designing and implementing can be adapted and applied to other educational and commercial applications. For example, other teaching and learning or training environments may include: surgery operations, civil and military services, visualisation for business, architecture and science, entertainment and others [5].

6 References

- [1] Esperan Ltd, 'Esperan MasterClass HDL Multimedia Tutorial', Ramsbury, <http://www.esperan.com>.
- [2] Stefan Sjöholm and Lennart Lindh, 'VHDL for Designers', Prentice Hall, 1997, ISBN 0-13-473414-9.
- [3] J. Vallino. 'Interactive Augmented Reality', *Phd Thesis*, Department of Computer Science, University of Rochester, New York, 1998, pp 1-25.
- [4] R. Azuma, 'A Survey of Augmented Reality', *Teleoperators and Virtual Environments*, 6, 4, 1997, pp 355-385.
- [5] J. Barrilleaux, 'Experiences and Observations in Applying Augmented Reality to Live Training', Peculiar Technologies, 3800 Lake Shore Ave., Oakland, CA 94610, <http://www.augsim.com/vwsim99/vwsim99.html>.
- [6] Lawrence J. Rosenblum. 'Mission Visualisation for Planning and Training', *IEEE Computer Graphics and Applications*, Vol. 15, No. 5, September 1995.
- [7] E. Jay, M. White, and P. F. Lister, 'The Virtual Design Educator: Realistic or Optimistic? An Approach to Teaching Design Virtually', *In Proceedings of the 7th National Conference on Product Design Education*, University of Sussex, Brighton, UK, 6-7 September 2000.
- [8] A. Kavassis, P. Watten, P. Lister and M. White, 'Virtual Prototyping of Electronics Systems', University of Sussex, <http://www.eeug.org.uk/sep00/abstract.htm#vprot>, EEUG Workshop, Sheffield University, September 2000.
- [9] Extensible Markup Language (XML) 1.0 (Second Edition), W3C Recommendation 6 October 2000, W3C XML Core Working Group, <http://www.w3.org/TR/2000/REC-xml-20001006>.
- [10] Lee Anne Philips, 'Using XML', Published by QUE, ISBN 0-7897-1996-7, August 2000.

- [11] Augmented Representation of Cultural Objects (ARCO), A Framework V Information Societies Technology proposal to the European Union, University of Sussex, December 2000.
- [12] Ben Chang, Mark Scardina, et al, 'Oracle XML Handbook', Osborne McGraw-Hill; ISBN: 007212489X.
- [13] M. Roussos, A. Johnson, J. Leigh, C. Vasilakis, C. Barnes, T. Moher. "NICE: Combining Constructionism, Narrative and Collaboration in a Virtual Learning Environment", Computer Graphics, Volume 31 Number 3 August 1997, A publication of ACM SIGGRAPH, pp 62-63.

List of Figures

Figure 8 Our current teaching model

Figure 9 Top down design flow

Figure 10 Areas where augmented reality could be used

Figure 11 Vertical teaching model

Figure 12 Horizontal teaching model

Figure 13 VITE system architecture adapted from the Oracle XML handbook

Figure 14 Augmented reality environment